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Question Paper Code : 91031

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2025.

Third Semester

Electrical and Electronics Engineering

EE 3302 – DIGITAL LOGIC CIRCUITS

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Calculate the BCD equivalent value for the gray number $(1110)_2$.
2. Determine the binary and decimal equivalent of $(FACE)_{16}$.
3. Simplify the following using De Morgan's theorem $\left[\left((AB)'C \right)'' D \right]'$.
4. State the absorption law of Boolean algebra.
5. Depict the state diagram of SR Flipflop.
6. Define race around condition.
7. Differentiate between asynchronous and synchronous sequential circuits.
8. What is a Self-starting counter?
9. Classify the datatypes supported by VHDL.
10. Write the VHDL code for basic two input AND gate.

PART B — (5 × 13 = 65 marks)

11. (a) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word readout is as

(i) 101110010100

(ii) 111111110100

Or

- (b) Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families.

12. (a) Simplify the Boolean function using K – map and implement using only NAND gates.

$F(A, B, C, D) = \sum m(0, 8, 11, 12, 15) + \sum d(1, 2, 4, 7, 10, 14)$. Mark the essential and non – essential prime implicants.

Or

- (b) Simplify the given Boolean function $F(A, B, C, D) = \sum(0, 1, 2, 5, 8, 9, 10)$ into

(i) Sum of products form

(ii) Product of sum form

Also implement both the forms using basic gates.

13. (a) Explain the various types of triggering with suitable diagrams. Highlight their merits and demerits.

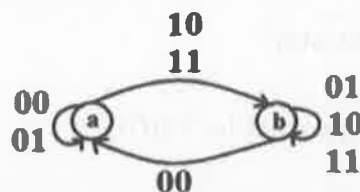
Or

- (b) Elaborate the steps involved in converting SR Flip-Flop to JK Flip-Flop.

14. (a) Derive the transition table and primitive flow table for the fundamental mode Asynchronous sequential circuits.

Or

- (b) Design an asynchronous sequential logic circuit for the state transition diagram shown in figure.



15. (a) Design a 3-bit magnitude comparator and write the VHDL code to realize it using structural modeling.

Or

- (b) Formulate VHDL code for the synchronous mod-6 counter with active low reset and set inputs.

PART C — ($1 \times 15 = 15$ marks)

16. (a) Minimize the following using k map. Implement the resultant function using NOR gates only. $f(A, B, C, D, E) = \pi M(2, 4, 7, 9, 26, 28, 29, 31)$.

Or

- (b) Design a 3-Bit Synchronous Binary Counter using JK flip-flop.

